# NeuroStack Hardware Manual



Version 1.9.2 Revised 08/24/2018



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# Contents

1	GET	TING STARTED	4
	1.1	WINDOWS	4
	1.2	Linux	4
	1.3	TEST WITH THE NEUROSTACK CONSOLE (WINDOWS ONLY)	5
2	HAI	RDWARE CONFIGURATION	6
	2.1	POWER SUPPLY	6
	Sou	rce Select (J13)	6
	24V	' Connector (J10)	6
	2.2	MASTER OR SLAVE CONFIGURATION	6
	Sing	gle board (default)	6
	Ma	ster board, or the base board of a stack of boards	6
	Sla	le board, or any stacked board which is not a master	6 ح
	2.3	USB VERSION	/
3	HAI	RDWARE DESCRIPTION	8
	3.1	COMPONENT OVERVIEW	8
4	COI	NNECTIVITY AND I/OS	9
	4.1	CONFIGURATION SWITCH (SW1)	9
	4.2	SPINE CONNECTORS	9
	Spir	ne connector North Top (J5) and North Bottom (J7)	9
	Spir	ne connector South Top (J6) and South Bottom (J8)	9
	4.3	CARDINAL CONNECTORS AND SWITCHES	10
	Car	dinal Connector	10
	Car	dinal Switch	10
	4.4	JTAG (J9)	11
	4.5	LEDS	11
5	PRC	OGRAMMING THE FPGA	12
	5.1	JTAG CONNECTION	12
	5.2	PROGRAMMING WITH THE DIAMOND PROGRAMMER TOOL	12
	5.3	PROGRAMMING WITH ISPVM SYSTEM SOFTWARE	14
6	RE-	PROGRAMMING THE FTDI USB CHIP	16
	6.1	Switch configuration	16
	6.2	PROGRAM THE FTDI USB CHIP	16
7	ME	CHANICAL AND ELECTRICAL SPECIFICATIONS	18
8	STA	CK ASSEMBLY	19
	8.1	JUMPER CONFIGURATIONS	19
	8.2	Instructions	19
	8.3	TROUBLESHOOTING	19

# **1** Getting Started

The NeuroStack interfaces to USB ports through a USB2 chip from FTDI. At factory default, the board is ready to use as a single board, powered through its USB port. If this is not your ordered configuration, verify the hardware settings described in paragraph 2.3 to 2.5. For details on the firmware configuration and the functions programmed in the FPGA, refer to the <u>NeuroStack Firmware Manual</u>.

### 1.1 Windows

- Connect the NeuroStack to the USB connector of your PC.
- Go to Settings/Device Manager
- If the NeuroStack is properly recognized, it will appear as a USB device named "USB Serial Converter" with "FTDI" as the manufacturer.
- Otherwise it will appear as Other devices/USB<->Serial Converter.
  - Right click and select Properties, then select the Driver tab and click the Install Driver button.
  - If not found automatically, go visit <u>http://www.ftdichip.com/Drivers/D2XX.htm</u> to download the driver compatible with your hardware.
- Test the proper connection to the board and access the NeuroMem CM1K chip with the NeuroStack Console application described below

#### Troubleshooting:

- The NeuroStack uses an FTDI USB chip commonly used in many USB devices. In case of trouble detecting the board, try unplugging the other USB devices to detect conflicts.
- Verify the jumper and dip switch settings described below

### 1.2 Linux

Connect the board and visit <u>http://www.ftdichip.com/Drivers/D2XX.htm</u> to download the driver XYZ compatible with your hardware.

>> tar xfvz libftd2xx-XYZ.tgz
>> cd build
>> sudo -s
>> cp libftd2xx.\* /usr/local/lib
>> chmod 0755 /usr/local/lib/libftd2xx.so.XYZ

Creates a symbolic link to the ABC version of the shared object >> In -sf /usr/local/lib/libftd2xx.so.A.B.C /usr/local/lib/libftd2xx.so

Verify that the USB connection to the board is established. The vendor and product ID should be 0403:6014. >> lsusb

To properly interface to the NeuroStack board

Start an interactive shell >> sudo -s >> export LD\_LIBRARY\_PATH=/user/local/lib

\_\_\_\_\_

To prevent another driver for the FTDI USB device from loading, you may have to unload "ftdi\_sio" and its helper module "usbserial" if they are installed >> sudo rmmod ftdi\_sio >> sudo rmmod usbserial

Verify that the USB connection to the board is established

>> Isusb

The NeuroStack should be identified as Bus 00x Device 0yz: ID 0403:6014 Future Technology Devices International, Ltd FT232H Single HS USB-UART/FIFO IC

Execute the simple script supplied with the board >> cd neurostack/examples\_c/app >> make >> ./simplescript

#### Troubleshooting:

- The NeuroStack uses an FTDI USB chip commonly used in many USB devices. In case of trouble detecting the board, try unplugging the other USB devices to detect conflicts.
- Verify the jumper and dip switch settings described below

### 1.3 Test with the NeuroStack Console (Windows only)

The NeuroStack Console software is compatible with a single board or a stack of boards and allows you to verify the proper connection to the board and access the NeuroMem CM1K chip and modules programmed in the FPGA through a simple Register Transfer Level protocol. These modules and registers are described later in this manual. For detailed information about the NeuroStack Console interface, refer to the <u>NeuroStack Console User's Manual</u>.

If you are using a stack of NeuroStack, the application will automatically size the neural network and let you verify that all boards are accounted for (4096 neurons per board). Note that this operation which runs at the launch of the program may takes a few seconds.

The modules and their registers are described in the <u>NeuroStack Firmware Manual</u>. For example, reading the register 6 (MINIF) of module 1 (CM1K) must return the value 2 at factory settings.

- Install the NeuroStack Console software
- Start the program from the Start menu/General Vision/NeuroStack Diagnostics
- The launch of the application triggers the sizing of the stack and may take up to 4 seconds per board
- Verify that the correct number of neurons is reported in the results box, or 4096 times the number of boards.
- Refer to the <u>NeuroStack Console</u> manual for further details or go directly to installation and use of a compatible Software Development Kit.

# 2 Hardware configuration

### 2.1 Power supply

A single board can be powered through USB power supply (default) or an external 24V external power supply. A stack of two or more boards must be powered by an external 24V external power supply.

#### Source Select (J13)

This jumper requires a jumper connector to be present for power to be delivered to the board. A Jumper across 1-2 sources power to the card from the USB connector (single board configuration only). A jumper across 2-3 sources power from the on board 24V to 5V Regulator.



#### 24V Connector (J10)

This header is a poke-home connector for connecting the board to an external 24v power supply. Insert strip wires into the bottom portion of the connector as described in the table below. To release a wire, push a pin in the upper hole while pulling the wire.

Pin #	Pin Name	GND 24v	24v Jumper Select
1 (+)	24V		<b>^</b>
2 (-)	Ground		

### 2.2 Master or Slave configuration

#### Single board (default)

Receives the external power supply, handles USB communication with the host and executes the functions
programmed in the FPGA and interfacing to the 4 CM1K chips of the board, seen as a single chain of neurons
or multiple chains of neurons.

#### Master board, or the base board of a stack of boards

 Receives the external power supply and propagates to the other boards, handles USB communication with the host and executes the functions programmed in the FPGA and interfacing to the CM1K chips of all the stacked boards, seen as a single chain of neurons or multiple chains of neurons. Propagation of the power lines and instructions for the stached CM1K chips is made through the spine connectors.

#### *Slave board*, or any stacked board which is not a master

- Receives its power supply and instructions for its 4 CM1K chips through the spine connectors.

For ease of use and flexibility, the default FPGA configuration file has been programmed to be the same for the three categories of boards. It relies on the settings of the dip switch SW1 to enable/disable the appropriate IP cores. For details on the default configuration and the functions programmed in the FPGA, refer to the <u>NeuroStack</u> <u>Firmware Manual</u>.

Single board (default)	Master board	Slave board
J13 1-2 or 2-3	J13 2-3	J13 2-3
SW1 pin7 low	SW1 pin7 high	SW1 pin7 high
SW1 pin8 high	SW1 pin8 low	SW1 pin8 high
SW2, pin 8 high	SW2, pin 8 low	SW2, pin 8 high

#### Single board





# 2.3 USB version

If you have an 1<sup>st</sup> generation of board with a dual-block power supply, the wiring of the USB port in the configuration file is slightly different. It can be selected through the pin 6 of the Configuration Switch SW1.

Current version has a single block power supply. Pin6 on SW1 is up.



Earlier versions have dual block power supply. Pin6 on SW1 must be down.



# 3 Hardware Description

#### 3.1 Component Overview



- Bank of four CM1K chips
  - At factory default, the configuration file connects the four CM1K chips in a daisy-chain of 4096 neurons extending to another chain of 4096 if another board is stacked.
  - o By reconfiguring the FPGA, the four CM1K chips can work independently from one another.
- Field Programmable Gate Array
  - o Lattice XP2 FPGA with 40,000 logic elements (Model LFXP2-40E, BGA 484 balls)
  - Programmable through a JTAG connector, USB connector or 2 SPI lines.
- FTDI USB chip
  - Single channel USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO IC. It has the capability of being configured in a variety of industry standard serial or parallel interfaces.
- Bank of MRAMs
  - Two 2 Mbytes (2M x16bits) MRAM, 35 ns access time

# 4 Connectivity and I/Os

### 4.1 Configuration switch (SW1)

The switch SW1 allows defining the configuration and operation of the board through external switch positions. The following table describes the use of these switches in the default configuration file.

Pin #	Pin Name	Pin Number	Pin Name
1	Unused	2	Unused
3	Unused	4	Unused
5	Unused	6	USB HW wiring version
7	Down, Single board	8	Down, Master board
	Up, Stackable board		Up, Slave board
9	Unused	10	Unused
11	Unused	12	Unused
13	Unused	14	Unused
15	Unused	16	Unused

#### 4.2 Spine connectors

The spinal connectors enable the vertical stack ability of the NeuroStack modules and the expansion of the neural network by connecting the CM1K chips from multiple boards on a same parallel bus. The top side connectors are 2 "spinal" spring-loaded 18-pin connectors. The bottom side connectors are simple pads mirroring the top connectors, except for the daisy-chain in (DCI) signal of J8 which becomes the daisy-chain out (DCO) signal on J6.

Warning: If you probe the signals of the spinal connectors J6 and J8, DO NOT short pins 1 and 2 which are the 24v VCC lines.

#### Spine connector North Top (J5) and North Bottom (J7)

Pin #	Pin Name	Pin Name	Pin Number
1	CMB_D00	CMB_D08	2
3	CMB_D01	CMB_D09	4
5	CMB_D02	CMB_D10	6
7	CMB_D03	CMB_D11	8
9	CMB_D04	CMB_D12	10
11	CMB_D05	CMB_D13	12
13	CMB_D06	CMB_D14	14
15	CMB_D07	CMB_D15	16
17	Ground	Ground	18

Spine connector South Top (J6) and South Bottom (J8)

Pin #	Pin Name	Pin Name	Pin Number
1	24V	24V	2
3	CMB_SP0	CMB_RDY	4
5	CMB_CSn	CMB_CLK	6
7	CMB_BSY	CMB_IDn	8
9	CMB_R0	CMB_UNCn	10
11	CMB_R1	CMB_DS	12
13	CMB_R2	CMB_RWn	14
15	CMB_R3	CMB_DCO for South Top (J6)	16
		CMB_DCI for South Bottom (J8)	
17	CMB_R4	CMB_RSTn	18

#### 4.3 Cardinal connectors and switches

Four configurable "cardinal" connectors allow interfacing the board to sensors and other I/O devices through LVDS, I2C, SPI or other communication bus.

Each board has four 8-pins push-in connector and four associated dip switches to define if the lines are singleended or differential pairs. A single connector can accept 3 differential pairs plus 2 single-ended wires, or eight single-ended wires. The lines of multiple connectors can be combined to define a bus of up to 32 single-ended lines.

	Connector	Configuration Switch	
North	J1	SW2	
East	J4	SW5	
South	J2	SW3	
West	J3	SW4	

or other signals.

The differential pairs can be LVDS. They require that the The single-ended wires can be used to connect I2C, SPI switch between their lines is closed.





#### **Cardinal Connector**

All four cardinal connectors have the following pin assignment:

Pin #	Pin Name
1	User defined, 3.3V
2	User defined, 3.3V
3	User defined, 2.5V
4	User defined, 2.5V
5	User defined, 2.5V
6	User defined, 2.5V
7	User defined, 2.5V
8	User defined, 2.5V

#### Cardinal Switch

The pin assignment of the four cardinal switches may defer slightly as described in the table below:

Pin #	Pin Name	Pin Name	Pin #
1	3.3V	I2C_SDA	2
3	3.3V	I2C_SCL	4
5	SO	SO <sup>(2)</sup>	6
7	S1 (2)	S1 <sup>(1)</sup>	8
9	S2	S2	10

11	No Connect	No Connect	12
13	No Connect	No Connect	14
15	No Connect	No Connect	16

<sup>(1)</sup> On the North switch (SW2) pin#8 is reserved to define if the pull-up resistors shall be enabled or not. Pin#8 must be down for the bottom and top boards of a stack.

<sup>(1)</sup> On the West switch (SW4) pin#8 is reserved to define the boot configuration of the FPGA

<sup>(2)</sup> On the North switch (SW2) pin#6-7 are reserved to enable the future programming of the FPGA via a USB connection without the need for a Lattice programming cable.

# 4.4 JTAG (J9)

- JTAG to program and debug the FPGA

Pin #	Pin Name	Pin Name	Pin #
1	JTAG_TDI	VCC (3.3V)	2
3	JTAG_TDO	No Connect	4
5	JTAG_TCK	No Connect	6
7	JTAG_TMS	No Connect	8
9	JTAG_TRST	Ground	10

#### 4.5 LEDs

Four sets of three LEDS are placed along the four edges of the board. Their functionality of defined by the configuration file programmed on the board.

# 5 Programming the FPGA

The FPGA of the NeuroStack can be programmed using Lattice's Diamond software which is available from the Lattice website and a Lattice USB JTAG programmer.

### 5.1 JTAG connection

- Connect NeuroStack to its power supply, whether through a USB port or an external supply.
- Connect the output leads of your programming cable to the corresponding pins of the JTAG connector (J9).

1 Revu	1	Õ		
8052	Ŀ	9		
COGNIN	D	C C	-	
		CC		
		Ge		
mmm	4	C.C	-	
minnin	110	21	Γ	

Pin #	Pin Name	Pin Name	Pin #
1	JTAG_TDI	VCC (3.3V)	2
3	JTAG_TDO	No Connect	4
5	JTAG_TCK	No Connect	6
7	JTAG_ TMS	No Connect	8
9	JTAG_TRST	Ground	10

### 5.2 Programming with the Diamond Programmer Tool

The files necessary to program a new configuration include a \*.jed file and a \*.xcf file. They are supplied in the folder FPGA\_Firmware\CBX\_Default.

Open the Diamond application and select the project saved in this folder and labeled CBX\_Default.ldf.



- Click at the Program icon ( 🏁 ) and wait until the operation is reported as successful.
- If the project does not load properly, the following definition steps might be necessary through a series of pop-up menus:
  - The model of FPGA on the NeuroStack board is an XP2 packaged in a BGA 484 balls.
  - The synthesis tool is SynplifyPro
- Click the Programmer icon in the toolbar or select it through the Tools menu:



Fill the next panel by clicking the "Detect Cable" button and selecting the file CBX\_vX.xcf in the folder CBX\_ConfigFiles.

Programmer: Getting Started
Select an Action:
Oreate a new Project from a Scan
Cable: USB   Port: EzUSB-0  Detect Cable
Create a new Blank Project
Open an existing Programmer Project
C:/Lattice_projects/CBX_Decooda/CBX_Decooda_v1/CBX_Decooda_v1.xcf
Import file to current implementation
C:/Lattice_projects/CBX_ConfigFiles/CBX_v3.xcf
OK Close

The last step is the selection of the associated jed file which is also stored in the CBX\_ConfigFiles folder.

🚯 Start Page 🛛 🕅 Reports 🖾 🦃 Programmer - CBX_v3.xcf * 🛛					
Device	Operation	File Name			
LFXP2-40E	FLASH Erase, Program, Verify				
	Reports 💽 🐼 Progra Device LFXP2-40E	Reports     Programmer - CBX_v3.xcf * [X]       Device     Operation       LFXP2-40E     FLASH Erase, Program, Verify			

Finally click at the Program icon ( 🎂 ) and wait until the operation is reported as successful.

The files necessary to program a new configuration include a \*.jed file and a \*.xcf file.

Install the Lattice ispVM software located on the CD in the folder BringUp\_firmware/Ispvm\_v18. For latest versions and more information you can refer to

http://www.latticesemi.com/products/designsoftware/ispvmsystem/index.cfm

Setup	×
Select Components Which components should be installed?	
Select the components you want to install; dear the components you do install. Click Next when you are ready to continue.	o not want to
Custom Installation	•
V Model300 Programmer	2.5 MB 🔺
App Notes and Data Sheets	5.5 MB
✓ ispVMEmbedded Version 12 Source Code	0.5 MB
SysCONFIG Embedded Version 1 Source Code	0.3 MB
Slave SPI Embedded Version 2 Source Code	0.8 MB
FPGA Loader Device Database	1.3 MB
ispCLOCK Family Device Database	0.1 MB
Lattice FPGA Device Database	37.7 MB
IVIIMachXO2 Family Device Database	1.3 MB
Current selection requires at least 116,582 KB of disk space.	
< <u>B</u> ack Next >	Cancel

Remark: In the list above, you can exclude the installation of the components listed after the Lattice FPGA Devices such as CPLD, ORCA, ispPAC, Digital Interconnect and SPLD devices.

During the installation, you will be prompted to choose the driver to install. Choose depending on the model of your programming cable (USC PC if you are using the Lattice programming cable model HW-USBN-2A). For more information you can refer to

http://www.latticesemi.com/products/developmenthardware/programmingcables.cfm?source=topnav

Launch the program ispVM System application. Under Options, select the Cable and I/O Port setup menu and click auto-detect. Click OK when the USB is found.

Cable and I/O Port Setup					
Cable Type: USB    Port Setting: EzUSB-0  Castom Port: 0x  NOTE: Auto Detect only works with parallel port and USB cables.  NOTE: Connecting the board's TRST (	( <u>Auto Detect</u> ) <u>QK</u> <u>Cancel</u> <u>Debug Mode</u> the Lattice				
not recommended. Instead, connect the board's TRST to Vcc. The parallel port on some PCs may not be able to hold a high during the programming, and may have glitches, interrupting programming. NOTE: The order of the USB Port Address (ezUSB-0, ezUSB-1,ezUSB-N) might change when the system is rebooted or when the USB cable is repetitively connected and disconnected.					
NOTE: If ispVM does not recognize the USB cable even after installing the LSC USB Port Drivers and rebooting, click here					
Troubleshooting the USB Driver Installation Guide.					
TRST/Reset Pin Connected     Set High     Set Low					
DONE Pin Connected	PROGRAMN Pin Connected				
INITN Pin Connected					

Under ispTools, select Scan chain. The Device List should report one LFXP2-40E device which is the model of FPGA on the NeuroStack board



Double click on the line LFXP2-40E to display the Device Information.

Edit a Part Description.

Under the Data File button, select Browse and find the location of the file CBX\_default.jed

		<u>0</u> K	
CogniBlox			
Device:		<u>C</u> ancel	
Select LFXP2-40E		 Advanced.	
Device Full Name:	Package:		
LFXP2-40E-XXF484	484-ball fpBGA	Expand	
Data File:			
Browse C:\CD_CBX\B	5		
Instruction Register Length:			
Import 8	Enable Debug Mo	in Program Error ode	
Import 8	E Re-initialize Part o	n Program Error ode	
Import 8 Operation: FLASH Erase,Program,Verify Device Access Options	Re-initialize Part of Enable Debug Model	n Program Error ode	
Import         B            Operation:	Re-initialize Part c	n Program Error ode	

Click OK and wait under the panel closes.

Click the Go icon to program the FPGA and wait until the process passes. This command can also be found under the Project menu. This takes approximately 30 seconds and the Status should report Pass.

Ū	🚺 LSC ispVM® System Version 18.0.2 - Chain configuration1*							
Eil	Eile Edit View Project ispIools Options Window Help							
~								
Ľ	🖷 Chair	n configuration1*						
	Index	Device List	FileName/IR-Length	Operation	Status			
	🀲 1	LFXP2-40E	C:\CD_CBX\BringUp_firmware\CBX	FLASH Erase, Program, Ve	PASS			
								ι απιςι
								Semiconducto
								Corporation
	Status							
Operation Done. No errors.								
	Operation: Successful							
ll I €						-		
Rea	dy							

# 6 Re-Programming the FTDI USB chip

The FTDI chip of the NeuroStack is programmed at the factory, so it should appear under the Control Panel/Device Manager as a USB serial converter and you should not need to ever proceed with the instructions given in this chapter.

The latter are supplied for reference anyhow.

#### 6.1 Switch configuration

- Select USB as the power supply
  - Place a jumper across pins 1-2 on J13
  - Set the board in a single board configuration
    - SW1 pin8 down (The board is a master board. It receives the communication from the host and propagates the instructions to the other boards through the spine connectors)

# 6.2 Program the FTDI USB chip

- Connect NeuroStack to the PC via its USB cable
- Install the FTDI console (located on the CD in AdvancedTools/NS4K FTDI firmware/FT\_Prog\_v24)
- Launch the program
- Click at the Scan icon in the main toolbar (  $\stackrel{
  ho}{\succ}$  )
- Go down the chain Device/FT EEPROM/Hardware Specific/Port A/Hardware and select 245 FIFO



- Go down the chain Device/FT EEPROM/Hardware Specific/Port A/Driver and select DX2XX

🕒 FTDI - FT Prog - Device: 0 [Loc ID:529]						
EEPROM W Rash ROM						
File Devices Help						
Device Tree	Property	Value				
□ 🚓 Device: 0 [Loc ID:529] □ → FT EEPROM	Vitual COM Port	0				
	D2XX Direct	۲				
Hardware	Information Box					
UART	Virtual COM Port / D2XX					
→ 245FIFO → CPUFIFO → OPTO → FT1248	The driver that is ins be set by selecting option.	talled and used by each channel can Virtual COM Port or D2XX Direct				
Driver → D2XX → VCP						
<ul> <li>➡ FT1248 Settings</li> <li>➡ IO Controls</li> <li>➡ IO Pins</li> </ul>	Device Output Read EEPROM Devic Word 0000: 0100 0304 1	e 0				

- Click at the Program icon in the main toolbar (  $\overset{\mathscr{I}}{\sim}$  )

Device List	Device Overview				
Device: 0 [Loc ID:529]	De	wice: 0 [Loc ID:529]			
	Chip Type:	'FT232H'			
	Vendor ID:	0x0403			
	Product ID:	0x6014			
	Manufacturer:	'FTDI'			
	Product Description:	USB <> Serial Converter			
	Serial Number:	FTV5SZM8 Auto-Generate			
Select All Deselect All	] [	Only Program Blank Devices			
Cycle Ports	-	<b>D</b>			

- Unplug, replug and verify that the device appears under the Control Panel/Device Manager as a USB Serial Converter.

# 7 Mechanical and Electrical Specifications



Dimensions

3"x3", ½" vertical spacers between stacked boards



# 8 Stack assembly

## 8.1 Jumper configurations

Single board (default)	Master board	Slave board
J13 1-2 or 2-3	J13 2-3	J13 2-3
SW1 pin7 low	SW1 pin7 high	SW1 pin7 high
SW1 pin8 high	SW1 pin8 low	SW1 pin8 high
SW2, pin 8 high	SW2, pin 8 low	SW2, pin 8 high

### 8.2 Instructions

- Prepare the boards to be powered by an external 24v power supply

   J13 set jumper between 2-3 pins
- 2. Prepare the master board
  - a. SW1, pin 8 low
  - b. SW2, pin 8 low
  - c. If old version of the board, SW1, pin 6 low (refer to chapter 2.3)
- 3. Prepare the slave board(s)
  - a. SW1, all pins high
  - b. SW2, all pins high
- 4. Using 8 male-female standoffs with a length of 10mm and a thread of 3 mm diameter, stack the slave board on top of the master board and tighten with 4 female-female standoffs or M3 Phillips screws.



- 6. Launch the NeuroMem console on your PC and select the NeuroStack hardware platform
- 7. Wait approximately 4 seconds per board while the Console is sizing the NeuroMem network
- 8. Verify that the number of reported neurons is equal to 4096 \* N neurons with N the number of boards in your stack.
- 9. Select the "Inter Chip" box and click the Run button. When the routine is finished, verify that all tests report a PASS
- 10. If applicable, disconnect the stack, add the next slave board and loop to 5

# 8.3 Troubleshooting

Make sure that all boards work correctly using the external power supply but configured a Single board:

- 1. Configure the board for Single mode
  - a. J13 set jumper between 2-3 pins
  - b. SW1, pin 7 low
  - c. SW1, pin 8 high
  - d. SW2, pin 8 high
  - e. If old version of the board, SW1, pin 6 low (refer to chapter 2.3)
- 2. Connect the board to the external 24v power supply and its USB connector to your PC
- 3. Launch the NeuroMem console on your PC and select the NeuroStack hardware platform
- 4. Verify that the number of reported neurons is equal to 4096 neurons
- 5. Select the "Inter Chip" box and click the Run button. When the routine is finished, verify that all tests report a PASS

